Docket No.: 21806-00156-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kiran Chatty et al.

Application No.: 10/605,699 Confirmation No.: 2698

Filed: October 21, 2003 Art Unit: 2818

For: METHOD AND STRUCTURE TO SUPPRESS EXTERNAL LATCHUP Examiner: David Vu

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is filed in response to the Examiner's Answer mailed November 27, 2006. More specifically the errors in the attribution of certain subject matter to the cited references of U.S. Patent No. 5,675,170 (Kim) and U.S. Patent No. 4,642,667 (Magee) involved in the rejections of claims 1-31. Appellant respectfully submits the Examiner's Answer has: (1) ignored subject matter specifically defined in the claims; (2) has alleged subject matter is disclosed in the references when it is not disclosed therein.

INTRODUCTION

Overview of Applicants' Claimed Invention

The present invention relates to a method and structure for protection against latch-up. Integrated circuits manufactured in accordance with the present disclosure feature well and substrate contacts of varying periodicity. Such a strategy enables maximizing the design of an integrated circuit as to the suppression of latch-up while concurrently optimizing available area on the chip allocable to circuit design. The method and structure of the present invention is particularly beneficial to protect against cable discharge events and other discharge occurrences prone to injecting large current densities into an integrated circuit.

Detailed Summary of Claimed Invention with Reference to the Disclosure

A detailed discussion below is cross-referenced to the Specification and Figures is provided below as published in U.S. Patent Application Publication US 2005/0085028A1 (i.e., this application).

The present invention is a CMOS semiconductor structure comprising: a substrate; and a plurality of circuit structures formed upon the substrate. At least one of the circuit structures of the present invention has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure*; and a plurality of contact regions that are inter-spaced at varying distances between said circuit structures (emphasis added).

A typical dual-well latch-up structure can be seen by referring to **FIGS. 2A** and **2B** of the application.[1] Specifically, **FIG. 2A** shows the formation of a latch-up structure that comprises parasitic bipolar junction transistors **Q1** and **Q2** with *associated* horizontal $\mathbf{R_{nw\text{-}h}}$, $\mathbf{R_{pw\text{-}h}}$ and vertical $\mathbf{R_{nw\text{-}v}}$, $\mathbf{R_{pw\text{-}v}}$ components of well resistance (emphasis added).[2] That is, as can be seen from **FIG. 2A**, the term "associated," in the context of the disclosure of this application, refers to components that are located within the semiconductor structure.

FIG. 6B illustrates a diagrammatical cross-section of a portion of an integrated circuit semiconductor structure having contacts **651** of varying periodicity in accordance with an

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[1] US 2005/0085028 at paragraph **[0013]**, lines 1-2.
[2] *Id.* at paragraph **[0013],** lines 2-5.

embodiment of the present invention.[3] For purposes of the disclosure of this application, elements that inject current into the IC are referred to as "injectors" and the location where an "injector" injects current is referred to as an "injection site."[4] In FIG. **6B**, the "injector" is represented by the ESD diode **652** that is located within the semiconductor structure and provides a forward-bias that injects carriers into the p-substrate **650** "injector site" when an overstress voltage is applied to *I/O pad* **653** (emphasis added).[5] Current at or near the "injection site" will have the highest density so contacts **651** near the ESD diode **652** will have the smallest periodicity, identified here as **L1**.[6] In addition, the periodicity **L4** is greater than periodicity **L3**, which is greater than periodicity **L2**, which is greater than periodicity **L1**.[7]

Further, **FIG. 6B** illustrates well **655** having contacts **651** connected to pad **656**.[8] When well **655** is an n-well, contacts **651** comprise n+ regions coupled to V_{dd} through pad **656**; when well **655** is a p-well, contacts **651** comprise p+ regions coupled to ground, or V_{ss}, through pad **656**.[9] The regions **654** between contacts **651** include structures that may be susceptible to latch-up.[10]

1. ***The anticipation rejection over Kim is deficient, as the applied art does not disclose all the limitations of claims 1-10 and 15-31.***

Kim discloses an apparatus for decreasing latch-up in I/O circuits such as a data output buffer.[11] In particular, Kim discloses an NMOS transistor is formed in the p-well **2**, and a PMOS transistor is formed in the N-well **3**. The NMOS transistor is composed of a gate electrode **21** and first and second N^+ regions **22** and **23** connected to a source and a drain electrode, respectively, located on the surface of the semiconductor structure. The first N^+ region **22** is connected to a grounded voltage source V_{ss} through the source electrode and the second N^+ region **23** is connected to a data input and output pad(Data I/O pad) **5** through the

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[3] *Id.* at paragraph **[0060],** lines 1-4.
[4] *Id.* at FIG. 4, paragraph **[0042]**, lines 1-4.
[5] *Id.* at paragraph **[0060],** lines 4 -7.
[6] *Id.* at paragraph **[0060],** lines 8 -11.
[7] *Id.* at paragraph **[0060],** lines 11-13.
[8] *Id.* at paragraph **[0061],** lines 1-2.
[9] *Id.* at paragraph **[0061],** lines 2-5.
[10] *Id.* at paragraph **[0061],** lines 5-7.
[11] Kim et al. ABSTRACT.

drain electrode located on the surface of the semiconductor. That is, in the context of the disclosure of the application, Kim disclose an "injector site" that is the drain electrode *located on the surface of the semiconductor device*.

In addition, Kim discloses an N-well guard ring **4** *that is disposed under a data input and output (I/O) pad* **5** (emphasis added).[12] Further, Kim discloses the N-well guard ring **4** is not only formed on a portion adjacent to the P-well **2** and the N-well **3**, but also formed on a portion of the P-type substrate *under the data I/O pad* **5**, wherein the N-well guard ring **4** is formed as a single enlarged N-well guard ring (emphasis added).[13]

However, Kim nowhere discloses, as recited in independent claim 1 and in similar language in independent claim 22:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

That is, in contrast to the claimed invention, Kim discloses a CMOS semiconductor structure wherein:

(1) the "injection site" is located on the surface of the semiconductor structure; and

(2) large n-well **4** is located beneath a data I/O pad **5**.

Further, it is respectfully submitted that Kim does *not* disclose: an apparatus with the "CMOS semiconductor structure" of the invention of claims 5 and 26. This is particularly apparent in comparing **FIG. 4** of Kim to **FIG. 6B** of the claimed invention and demonstrated in the language of dependent claims 5 and 26, which recite:

> forming a plurality of contact regions interspaced a varying distance between said circuit structures,

[12] *Id.* at FIG. 3, FIG. 4, column 2, lines 51-53.
[13] *Id.* at FIG. 3, FIG. 4, column 2, lines 53-56.

> *wherein said distance varies with the proximity of said plurality of contact regions to said injection site,*
>
> wherein said plurality of contact regions comprises a first contact region and a second contact region spaced a first distance apart, and said second contact region and a third contact region spaced a second distance apart different from said first distance.
>
> *wherein said first distance is greater than said second distance* (emphasis added).

That is, in the claimed invention, the "distance varies with proximity" (i.e., increases) as one moves away from the "injection site" (i.e., as stated above: "the periodicity **L4** is greater than periodicity **L3**, which is greater than periodicity **L2**, which is greater than periodicity **L1**"). In contrast, in **FIG. 4** Kim discloses the distance between electrode contacts **41, 32, 33, 34,** decreases as one moves away from the "injection site." Thus, Kim does not disclose the invention of claim 5. In addition, it is respectfully submitted that the outstanding Office Action and the Examiner's Answer is silent regarding the limitations of claims 6 and 27. Thus, the Office Action does not reject claims 6 and 27.

Furthermore, Kim discloses a "CMOS semiconductor structure" with multiple N-wells **3**, **4**. Moreover, in contrast to Kim, the structure of the semiconductor of the claimed invention is a single N-well 655. That is, the semiconductor structure of Kim teaches away from the semiconductor structure of the claimed invention.

Therefore, at least for the reasons above, it is respectfully submitted that Kim does not disclose, anticipate or inherently teach the claimed invention and that claims 1, 5, 6, 19, 26, 27, and claims dependent thereon, patentably distinguish thereover.

2. The anticipation rejection over Magee is deficient, as the applied art does not disclose all the limitations of claims 1, 7 and 11-14.

Magee discloses a bipolar lateral transistor that was compatible with "current NMOS or CMOS processing."[14] It should be noted that "current" at the time of the Magee patent disclosure was 1987. In particular, Magee discloses an npn lateral transistor structure that is

[14] Magee at ABSTRACT and column 2, lines 29-35.

formed in a very lightly doped p^{--} -type silicon substrate **11**.[15] In addition, Magee discloses a lightly doped n^- -type well **12** that is deeply diffused into the substrate **11** and a further lightly doped p^- -type well **13** that is diffused into the n^- -type well **12**.[16]

Further, Magee discloses a p-type region **14** that is diffused to form the intrinsic base, together with a p^+ -type region to act as a base contact.[17] Furthermore, Magee discloses that N^+ regions are added for the emitter **16** and collector contact region **17**, during which the emitter is diffused through the same window as the base **14**, to end up with a narrow P region surrounding and self aligned to the emitter. Moreover, Magee discloses the contact region **17** provides a collector for lateral transistor action and a collector contact for vertical transistor action.[18]

Moreover, Magee discloses the arrangement shown in **FIG. 2** comprises an n-channel **31** and p-channel **32** device each disposed in its respective n^- -type well **33** and **34**.[19] Further, Magee discloses for his invention that *devices of only one polarity*, e.g. NMOS transistors, may be employed. Furthermore, Magee discloses that in such a case, and where latch-up is not a problem, the n-channel transistor n^- -type well **33** is also not required. Magee also discloses advantageously a further p+ -type region **35** may be provided between the two complementary transistors **31** and **32** which zone is connected to the V_{ss} supply of the circuit. Magee also discloses a similar n+ -type region **36** in the n-channel transistor well is coupled to the V_{DD} supply.[20]

However, Magee nowhere discloses, as recited in independent claim 1 recites:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure;* and a

[15] Magee at column 1, lines 62-64.
[16] Magee at column 1, lines 64-66.
[17] Magee at column 1, lines 66-68.
[18] Magee at column 2, lines 5-7.
[19] *Id.* at column 2, lines 38-39.
[20] *Id.* at column 2, lines 49-50.

plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

That is, in contrast to the claimed invention, Magee discloses a CMOS semiconductor structure wherein:

(3) the "injection site" is located on the surface of the semiconductor structure; and

(4) large n-well **4** is located beneath a data I/O pad **5**.

In addition, Magee nowhere discloses as, claim 1 recites: "a plurality of contact regions inter-spaced a varying distance between said circuit structures." In particular, Magee discloses two circuit structures **31** and **32** but does not disclose a plurality contact regions **35, 36** "spaced a varying distance between said circuit structures."

Therefore, at least for the reasons above, it is respectfully submitted that Magee does not disclose, anticipate or inherently teach the claimed invention and that claim 1, and claims dependent thereon patentably distinguish thereover.

Conclusion

For the above-discussed reasons, as well as those provided in the Appeal Brief, Appellant requests reversal of the rejection of claims by the Honorable Board and allowance of pending claims 1-31 is respectfully requested.

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Respectfully submitted,

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